AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A delay-locked loop circuit[[,]] ~~comprising~~ comprising:

input means for an input signal that is to be delayed, said input means comprising means for splitting said input signal into a first and a second branch~~,~~;

~~where the signal in the first branch is connected to~~ a component for delaying the signal in the first branch;

the second branch being configured whereby ~~and~~ the signal in the second branch is used as a non-delayed reference signal for ~~the~~ a delay caused by the delay component in the first branch~~, characterized in that~~;

wherein the delay component ~~is~~ comprises a passive tunable delay line comprising an electrical conductor supported by a dielectric material~~, with the circuit comprising~~;

tuning means for the tunable delay line, said tuning means being affected by said reference signal~~, and with~~;

wherein the first branch ~~comprising~~ comprises output means for outputting a delayed signal with a chosen phase delay.

2. (Previously Presented) The circuit of claim 1, in which the delay component is continuously tunable.

3. (Previously Presented) The circuit of claim 1, in which the delay component is a passive component.

4. (Previously Presented) The circuit of claim 1, in which the delay component is a tunable ferroelectric delay line.

5. (Previously Presented) The circuit of claim 1, in which the second branch comprises a phase detector, by means of which the non-delayed signal of the second branch is compared to the delayed signal in the first branch at a point in the first branch where the delay to be caused by the delay component is known, the output signal from the phase detector being used as a control signal for the tuning means for the delay component of the first branch.

6. (New) The circuit of claim 1, wherein the delay component ~~is~~ comprises a ground plane which supports the dielectric material, and wherein a control signal applies a voltage between the electrical conductor and the ground plane to alter a dielectric constant of the dielectric material.

7. (New) The circuit of claim 1, wherein the delay component comprises plural signal phase take off points, wherein the plural signal phase take off points have differing phase shifts relative to one another, but wherein a phase shift at each take off point remains the same regardless of wavelength of the input signal.

8. (New) A delay-locked loop circuit comprising:

a splitter configured to split an input signal that is to be delayed into a first branch and a second branch;

a component for delaying the signal in the first branch, the delay component comprises a passive tunable delay line comprising an electrical conductor supported by a dielectric material;

the second branch being configured whereby the signal in the second branch is used as a non-delayed reference signal for a delay caused by the delay component in the first branch;

a tuner configured to tune the delay line in accordance with the reference signal.

9. (New) The circuit of claim 8, in which the delay component is continuously tunable.

10. (New) The circuit of claim 8, in which the delay component is a passive component.

11. (New) The circuit of claim 8, in which the delay component is a tunable ferroelectric delay line.

12. (New) The circuit of claim 8, in which the second branch comprises a phase detector, by means of which the non-delayed signal of the second branch is compared to the delayed signal in the first branch at a point in the first branch where the delay to be caused by the delay component is known, the output signal from the phase detector being used as a control signal for the tuner for the delay component of the first branch.

13. (New) The circuit of claim 8, wherein the delay component comprises a ground plane which supports the dielectric material, and wherein a control signal applies a voltage between the electrical conductor and the ground plane to alter a dielectric constant of the dielectric material.

14. (New) The circuit of claim 8, wherein the delay component comprises plural signal phase take off points, wherein the plural signal phase take off points have differing phase shifts relative to one another, but wherein a phase shift at each take off point remains the same regardless of wavelength of the input signal.